A DDS clock measurement module

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BIOGRAPHY

Mr. Riley has worked in frequency control his entire professional career. He is currently the Proprietor of Hamilton Technical Services, where he provides software and consulting services in that field. He was Manager of Rubidium Technology at Symmetricom (now Microsemi) and the Engineering Manager of the Rubidium Department at EG&G (now Excelitas) where he directed the design of rubidium frequency standards, including those used onboard the GPS satellites. He has BSEE and MSEE degrees, and has published a number of papers and tutorials. He is a Fellow of the IEEE, received the 2000 IEEE International Frequency Control Symposium Rabi Award and the 2011 Distinguished PTTI Service Award.

ABSTRACT

This paper describes a new method for making high-resolution phase measurements based on the use of phase control of a direct digital synthesizer (DDS). The technique can be implemented in the form of a small, simple USB-powered module and used to evaluate the performance of precision clocks and oscillators. Evaluation hardware, firmware and software are described that were used to validate the measurement concept, and have led to the development of a low cost module the size of a pack of cards that makes picosecond-level clock measurements when connected to a 10 MHz reference and a PC via a standard USB serial port interface. The device operates automatically at any frequency between 5 and 15 MHz, has a resolution of 6.1 ps at 10 MHz, and can acquire data at rates of 1 and 100 points/second. It can also be used as an 11 digits/second frequency counter. The module has a noise floor of about 1.3×10^{-11} at one second that decreases as the averaging time down to a floor below 1×10^{-15}, and it can track frequency changes as large as about 3×10^{-8}/second.

INTRODUCTION

Precise clock measurements are fundamental to the time and frequency field, and there is a continuing need for making these measurements using inexpensive and easy-to-use hardware. Many techniques have been devised for doing so, including high resolution time interval counters (TIC), dual mixer time difference (DMTD) systems and, more recently, digital techniques similar to software defined radios (some using cross-correlation). This paper presents a new approach, suggested to the author by Mr. Tom Van Baak at the 2014 PTTI meeting [1], which uses phase control of a DDS chip in a microprocessor-controlled phase tracking loop as a way to make high-resolution phase measurements. The technique compares the phase of the signal under test against a reference signal from the DDS at the same nominal frequency in an analog phase detector. The sense of the phase detector output is detected by an analog comparator whose 1-bit output steers the phase of the DDS via the microprocessor. A photograph of the module is shown in Figure 1; it is only about 1" high x 2" wide x 3 ½' deep and is powered by its USB interface.

Figure 1. DDS Clock Measurement Module

A conceptual block diagram of the basic system is shown in Figure 2. The phase tracking loop of the DDS clock measurement system keeps the phase detector centered at quadrature and uses the DDS phase word to produce a phase data stream to a USB port. The phase comparator information is also used to make DDS frequency adjustments as required to maintain phase tracking.

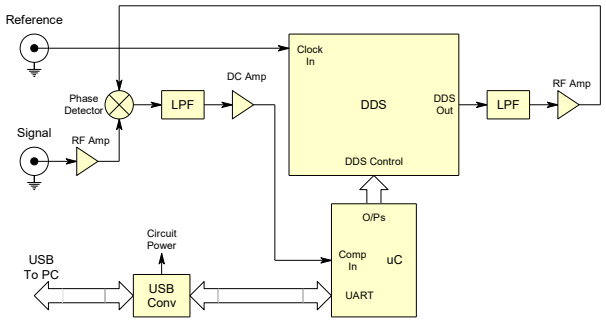

Figure 2. DDS Clock Measurement Module Conceptual Block Diagram

At 10 MHz, a DDS chip with 14-bit phase control has a resolution of about 6.1 ps that provides a quite useful measurement capability. That resolution is adequate for measuring the vast majority of frequency sources (e.g., most crystal oscillators and atomic frequency standards) as the quantization noise improves with averaging time. Furthermore, because the phase control loop can operate quite fast (e.g., 2.5 kHz), data can be streamed at high sampling (e.g., 100 points/second). The system can also be used as a high-resolution (11 digits/second) frequency counter.

CLOCK MEASUREMENT HARDWARE

The basis of the clock measurement hardware is a DDS chip with high-precision phase control, for example the Analog Devices AD9951 device used in the module described herein [2]. A block diagram of the AD9951 is shown in Figure 3. The DDS works by incrementing its phase accumulator by the frequency word at each clock cycle and the resulting phase value is transformed to a cosine function which is then converted into analog RF form by a DAC. For our purposes here, the critical thing is that a 14-bit offset can be added to the phase value, thereby adjusting the phase of the RF output. At 10 MHz, this corresponds to a phase resolution of 100 ns/2^{14} = 6.10 ps. Even higher phase resolution (0.2 ps) would be possible by expanding the width of the phase offset word to the full 19-bit width of the cosine conversion, something that might be possible with a future DDS device or FPGA.

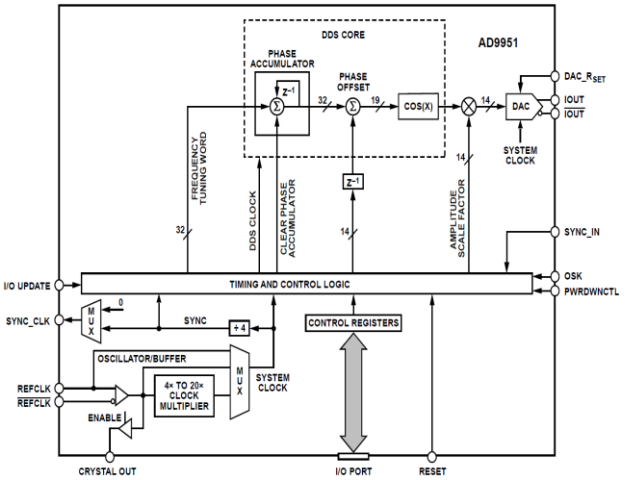

Figure 3. Block Diagram of the AD9951 DDS

The DDS also provides an adjustable frequency, of course, which needs to have adequate range to match the signal frequency and must have adequate resolution to limit the size of the phase slew caused by the finite offset between the DDS and signal frequencies. For example, near 10 MHz for a 32-bit DDS clocked at 120 MHz, the maximum frequency error is about 14 mHz or 1.4×10^{-9}. At exactly 10 MHz, the frequency offset is -9.31×10^{-10}, which corresponds to a phase slew of 931 ps/s or 153 DDS phase increments per second. This phase ramp must be removed by the instrument's software. An obvious way to improve this factor is to use a DDS with more frequency control bits.

The phase resolution also varies with the RF frequency. At 5 MHz it becomes x2 worse, 12.2 ps, and at 15 MHz it becomes 4.07 ps. One way to improve the phase resolution would be to use a higher DDS frequency and divide it down to the signal frequency. That works because the DDS phase increment is preserved through the divider. That method is limited by the frequency range of the DDS. For the AD9951, the resolution of a 10 MHz measurement could be improved by a factor of 5 by clocking the DDS at its maximum 180 MHz and operating it at 50 MHz.

The DDS is controlled by a Microchip Technology PIC16F1847 microcontroller [3]. That device has sufficient speed, program and RAM memory, I/O pins and features (UART, comparators, ADCs, timers, etc.) for this application. Its main functions are to automatically set and maintain the correct DDS frequency, to acquire phase lock and track the phase detector variations with the DDS phase control, and to communicate with a PC user interface application.

The 10 MHz reference input is divided by 4000 to produce a 2.5 kHz interrupt rate that determines the sampling rate of the phase tracking and data stream tau. The 10 MHz signal is also used to determine the gate time of a 1 second coarse signal frequency measurement, and counted for the duration of a nominal 100 Hz phase detector beat period measurement for a fine signal frequency measurement with a resolution of 10 mHz (1pp10^9 at 10 MHz).

DETAILED BLOCK DIAGRAM

A more detailed block diagram of the DDS Clock Measurement Module is shown in Figure 4. All circuits are powered from USB interface. Besides that 5V supply, the USB converter has a 3.3V regulator, and two additional 1.8V regulators supply the DDS chip. The 10 MHz reference input is split to clock the DDS, drive the 2.5 kHz divider and provide a clock for the PIC Timer0. The signal input is buffered and connected to one input of the phase detector; it also drives a digital comparator that produces a clock for the PIC Timer1. The other phase detector input is driven by the DDS output after low pass filtration and amplification. Power is removed from both digital comparators when not needed to reduce noise. The phase detector output, after low pass filtration, is amplified by two op amps, one feeding the PIC ADC input and the other its analog comparator.

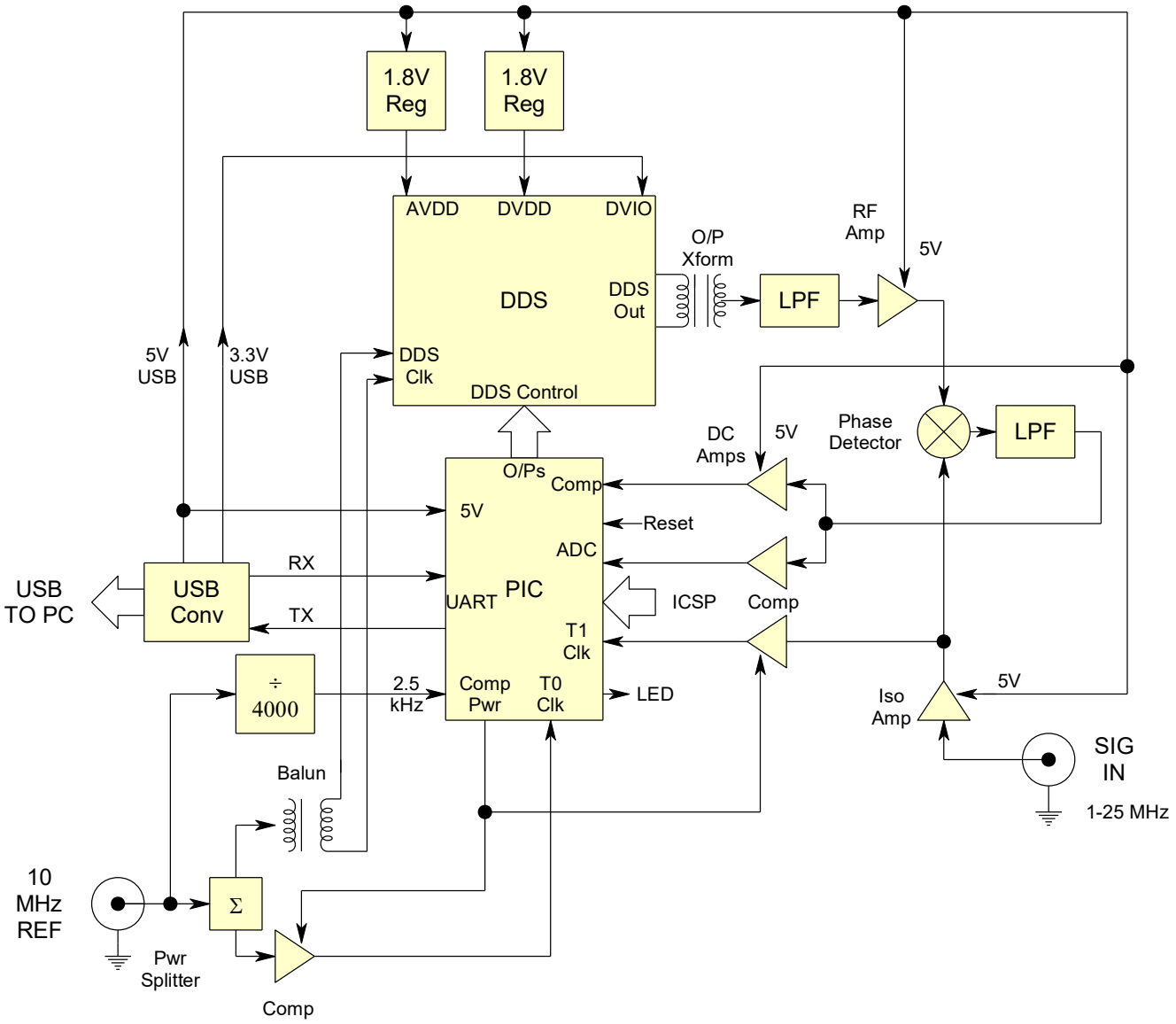

Figure 4. DDS Clock Measurement Module Detailed Block Diagram

The DDS section contains the DDS synthesizer with its reconstruction low pass filter, the PIC microcontroller and the USB interface converter. The PIC is programmed via its in-circuit programming (ICSP) interface. A reset switch and a monitor LED are also included. A jumper isolates the Timer1 clock input from the ICSP interface. The DDS reconstruction filter is a 7-section, 1 dB, 50 ohm elliptic low pass filter with a 15 MHz cut-off frequency, designed to have an attenuation of 60 dB above 18 MHz.

The RF section contains RF amplifiers for the signal under test and reference signals, the phase detector and its low pass filter, two DC amplifiers and the signal comparator. The phase detector and DC amplifiers are biased at +1.65 VDC, as is the PIC analog comparator. A test point is provided for the phase detector output.

The reference section accepts a 10 MHz sinewave signal at a nominal level of +7 dBm and splits it to clock the DDS differentially, drive a comparator to provide a reference squarewave to the PIC Timer0 input, and drive another PIC device that divides it by 4000 to produce a 2.5 kHz coherent sampling rate.

The power section contains two +1.8 V linear regulators for the DDS DVdd and AVdd supplies.

CLOCK MEASUREMENT FIRMWARE

The PIC16F1847 microcontroller firmware implements a main loop that checks for commands from the USB user interface, and an interrupt-driven process that periodically reads the state of the phase detector comparator and adjusts the DDS phase to maintain quadrature while sending phase data to the PC for time-tagging, capture and analysis. Means are also provided for initially measuring the signal frequency, setting the DDS frequency, acquiring phase lock, and various housekeeping functions. The DDS frequency is set as closely as possible to that of the signal under test so as to minimize the phase ramp rate, either automatically or according to a user-entered value. It is essential that the phase remain within one carrier cycle during a tracking update interval. All firmware calculations are performed in integer form without any floating-point usage, with the more complicated calculations done on the host PC.

The user interface commands are ASCII letters followed by =, ? or ↵ characters to denote setting, getting or displaying a parameter. Five output data formats are supported at rates of either 100/s or 1/s.

The output streams provide several formats to best support various measurement situations. The most complete provides incremental phase and frequency adjustment counts along with a phase correction associated with the frequency adjustment at a 1/s rate. Two 100/s data streams provide either signed decimal phase increments or both phase increment and frequency adjustment counts. Another provides a 100/s continuous stream of incremental phase bytes. Still another provides the absolute DDS phase word at a 1/s rate. At 10 MHz, each phase increment corresponds to 6.1 ps and, for a 1/s data stream, a fractional frequency increment of 6.1×10^{-12}. Because the phase tracking loop makes adjustments of ±1 count, they have only odd values that vary by 2.

PHASE TRACKING ALGOGITHM

The phase tracking algorithm keeps the phase detector at its center by correcting the phase of the DDS reference signal. It uses an analog comparator to sense the polarity of the phase detector output, producing a 1-bit response that is read at each 400 μs interrupt cycle, accumulating ±1 counts over a 25-cycle interrogation period. At the end of this 10 ms period the phase tracking algorithm makes a 1 LSB DDS phase correction in the direction to reduce the phase error. That process occurs regardless of the magnitude of the count, dithering the phase to eliminate any dead zone.

Without noise or frequency offset, the system toggles between two phase states. Noise changes that uniform alternation, and frequency offset introduces a bias that produces a systematic phase change in one direction. The algorithm works satisfactorily as long as the phase corrections are large enough to track the phase variations. Phase counts at the ±10 limit are an indication that the dynamic range is exceeded. A large frequency offset causes large phase counts to occur in the same direction while high noise causes them in both directions. The system must make DDS frequency adjustments to handle the former, and could use larger than 1 LSB phase corrections to handle the latter.

The relations between phase detector output voltage, comparator response and hysteresis, the interrogation period phase count and the amount of phase error is imprecise, but the measurements are precisely quantified by the 1 LSB DDS phase control sensitivity which is constant in degrees (360/2^14= 0.022°) and calculable in picoseconds knowing the nominal RF carrier period. The average phase change over any time interval depends on frequency offset and variation around that slope represent the noise. For the nominal phase detector sensitivity of 35 ps/mV, the comparator must have noise and hysteresis below about 175 μV, which necessitates amplification between the phase detector output and comparator input.

FREQUENCY AND PHASE ACQUISITION

Acceptable initial DDS frequency and phase settings are required for the DDS clock measurement module to operate properly and their acquisition can be accomplished as follows:

1. Either the operator must enter the nominal signal frequency to within a tolerance of about ±20 Hz (2 ppm at 10 MHz) or the module must obtain that information automatically. This quite a coarse tolerance and it is usually possible for the operator to satisfy it while by entering the nominal frequency to be used for calculating fractional frequency deviations, along with other parameters such as the desired data tau and the name of the data file.
2. If an automatic coarse determination of the signal frequency is needed, the module does so first by making an ordinary 1-second frequency counter measurement with respect to the 10 MHz reference.
3. The coarse signal frequency value is then used to set the DDS frequency so as to establish a nominal 100 Hz beat note at the phase detector output. The module then makes a period measurement of the beat frequency, which determines the signal frequency to within about 10 mHz (1×10^{-9} at 10 MHz). That value is then used to set the DDS very close to that of the applied signal, within ±1 DDS tuning increment. A final adjustment can be made to set the DDS exactly at the closest either by the operator or the module's frequency tracking loop, but that is not necessary.

4. The system must then acquire the proper quadrature phase condition before measurements can be made. While that will happen by means of the normal phase tracking process, it can be made faster by first using larger phase increments.
5. Phase lock can be verified by observing the phase detector output voltage, which must be stable and very close to its center value (the comparator DC reference voltage). The unit is then ready to start making measurements.

PHASE AND FREQUENCY TRACKING

During the measurement process, the module must track the signal phase variations and possibly make DDS frequency adjustments as follows:

1. In the absence of noise and frequency offset, the phase tracking loop alternates between plus and minus one DDS phase increment, two increments peak-to-peak. This would generate phase data that are either all odd or even values. Each increment is equal to the DDS signal period divided by 2^N, where N is the number of DDS phase control bits. For the AD9951 at 10 MHz, this is 100 ns/2^{14} or 6.10 ps.
2. Frequency offset introduces a phase ramp, and the tracking increments would be biased in one direction accordingly. For example, a frequency offset $1x10^{-9}$ would cause a phase ramp of 1 ns/s. The phase tracking loop must operate at a fast enough rate that the phase increments can keep up. At a 2.5 kHz sampling rate, one phase increment per sample can track a phase ramp of about $1.5x10^{-8}$ s/s at 10 MHz. So it is necessary to have means for making DDS frequency adjustments when the frequency offset exceeds a few pp10^9.
3. The need for a DDS frequency adjustment can be detected by the phase increments that exceed a certain rate. When a frequency adjustment is made during a measurement tau interval, the system must apply a phase correction to account for when it was made during the interval so that the transition is as seamless as possible.
4. Thus the complete data stream must include for each tau interval (a) the net number and polarity of phase increments, (b) the net number and polarity of frequency adjustments, and (c) a phase correction value to account for when the frequency adjustments were made during the interval.
5. Several other data formats are also desirable. If no frequency adjustments are enabled, only the phase increment data are needed. Those data can take the form of signed decimal values, signed integer hex characters, or single binary bytes. The data can be provided at rates as fast as the phase tracking loop or at longer multiples thereof (e.g., 1 second). No phase correction value is necessary for frequency adjustments at the fastest sampling rate.
6. The raw data stream is then processed by the user interface software to produce the final measurement results. That processing includes scaling the phase increments, removing the DDS frequency offset, applying frequency adjustments and their associated phase corrections, and time tagging the data. The user interface software is also responsible for controlling the system, displaying the results and saving them to a file and optional database for further analysis.

A flowchart of the phase and frequency tracking process is shown in Figure 5. Without a frequency offset, the DDS phase tracking corrections vary with the amount of source phase noise from small alternating corrections at the quantization level for low noise to larger corrections for more noise. With a frequency offset, the phase corrections are biased in one direction, and if large enough, a DDS frequency adjustment may be necessary to maintain phase tracking.

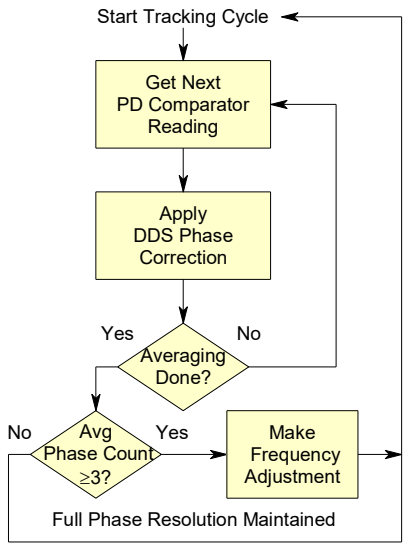

Figure 5. Phase and Frequency Tracking Flowchart

Operation at large noise levels was simulated by applying random noise to the tuning input of an OCVCXO, as shown in Figure 6. The ADEV was about $1x10^{-9}$, near the phase tracking limit without frequency adjustments.

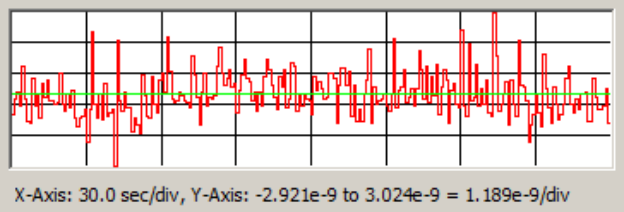

Figure 6. Frequency Record with Simulated Noise

Operation with frequency adjustments was simulated by applying a step voltage to the OCVCXO tuning input, with an RC filter to establish the initial slope, as shown in Figure 7. The frequency slew of 2.6×10^{-7}/s is near the limit without losing lock. Unlocking due to excessive frequency slew rate is a fundamental limitation of the DDS clock measurement concept.

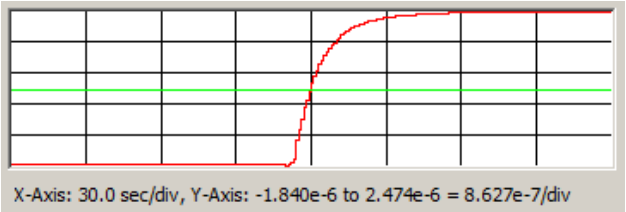

Figure 7. Frequency Record with Simulated Freq Slew

FIRMWARE OPERATION

The DDS clock measurement module firmware implements a main loop that checks for commands from the USB interface while responding to periodic interrupts to perform the measurements, as shown in the flowchart of Figure 6.

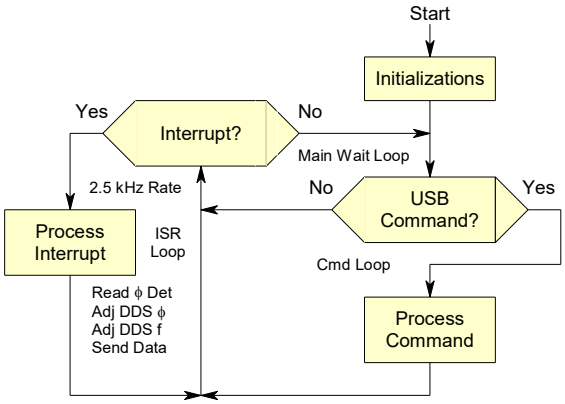

Figure 6. Firmware Flowchart

The interrupt-driven measurements are divided into twenty-five 400 µs cycles, each able to perform an operation such as sending data to the DDS or USB interface within its time slot. The phase detector state is sampled and the DDS phase is incremented or decremented accordingly at each interrupt cycle. These phase adjustments are summed over 25 cycles to produce an optional 10 ms data stream. The net phase adjustment over ten of those intervals is used to make any necessary frequency adjustments. Those phase and frequency adjustments, along with a phase correction for any frequency adjustments, are sent by the 1-second data stream.

MODULE PACKAGING

The DDS clock measurement module is implemented on a single 2-layer 50mm x 80mm circuit board as shown in Figure 7. It uses surface mount components and it requires no hand wiring, adjustments or calibration. The board then slips into its extruded aluminum case.

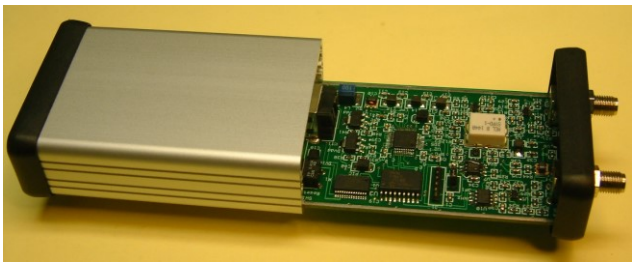

Figure 7. Clock Measurement Module Package

USER INTERFACE

The clock measurement module PC user interface software controls the measurement module, captures its data stream, displays the phase or frequency data, performs basic analysis and launches Stable32, TimeLab or another such program for more extensive analysis.

A screen shot of the main screen is shown in Figure 8. It can show a data listing or a plot of either the phase or frequency data. A separate configuration screen is used to set various module parameters. The user interface stores the timetagged phase data to a disk file, and can also store them in a PostgreSQL database.

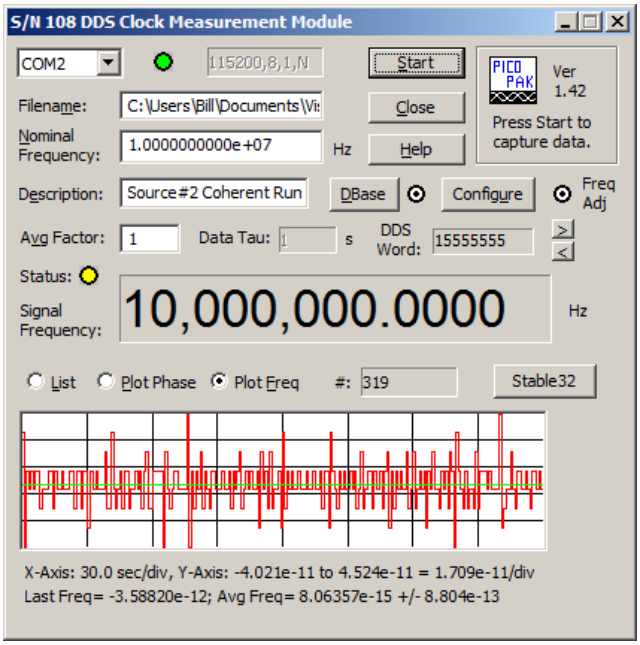

Figure 8. Main User Interface Screen

NOISE FLOOR

The typical noise floor of the DDS clock measurement module is shown in Figure 9. The dominant noise is white PM quantization noise that improves with longer averaging times from about 1.3×10^{-11} at 1 second down to the mid $pp10^{16}$ range at several hours.

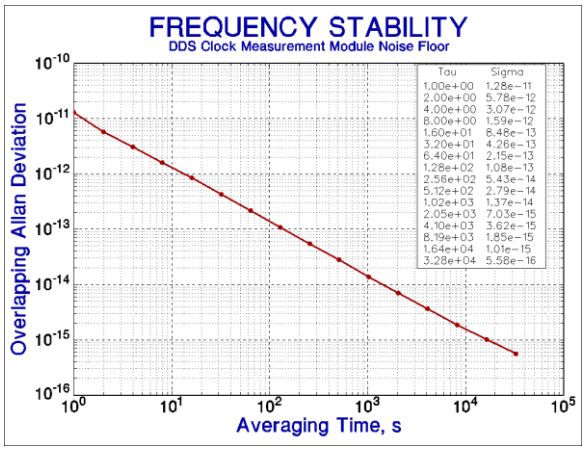

Figure 9. Clock Measurement Module Noise Floor

TEMPERATURE COEFFICIENT

Temperature sensitivity can be an important but often neglected aspect of a clock measuring system, causing its phase reading to vary with temperature and its frequency reading to vary with the rate of temperature change. The DDS clock measurement module has a typical TC of about 5 ps/°C, which is typical of such devices and not a severe problem in a laboratory environment.

DESIGN OPTIONS

Several options are possible for the DDS clock measurement concept as follows:

Digital Phase Detector: It is feasible to use a digital phase detector such as an Ex-OR gate instead of the analog one. That would be less expensive, and allow circuit simplification and a higher degree of integration. But phase-coherent interference generated by the digital signals could be a noise issue.

Higher Resolution: Higher resolution could be obtained most simply by using a DDS device having a larger number of phase control bits. It could also be realized by operating the DDS at a multiple of the signal frequency and dividing down its output by the same ratio to drive the phase detector. It might be necessary to also reduce the noise floor to achieve better performance, in part by using a low jitter VHF DDS clock source instead of employing its internal clock multiplier.

Two-Channel Cross-Correlation Measurements: Two modules can be used together to make simultaneous measurements to support cross-correlation processing as way to reduce the noise floor. One effective way of doing that is to capture time-tagged data at a higher rate (e.g., 100 Hz) and use their timetags to align the two data sets for analysis at a lower rate (e.g., 1 Hz), thereby avoiding the need to precisely synchronize the two devices. A noise floor improvement of around x5 has been obtained by this methodology.

Dual and Multi-Channel Configurations: A dual channel version of the DDS clock measuring module would be a useful configuration, as shown in Figure 10. A dual DDS (e.g., AD9958) could be used, and one processor could handle the two channels alternately. Such a configuration would be particularly appropriate for measuring two (possibly non-standard) frequency sources against each other. By taking their phase differences, the DDS clock would not have to be accurate, and a low noise free running VHF crystal oscillator could be used, along with an accurate 10 MHz "tau" reference clock driving the PIC timer. With a DDS clock derived from the 10 MHz reference, two signals can be measured or cross-correlation data obtained.

Multi-channel versions of the DDS clock measurement module would obviously also be feasible. Some economy could be realized by shared circuitry and a common package.

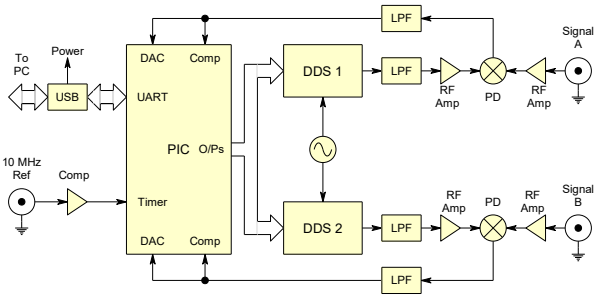

Figure 10. Dual-Channel Configuration

APPLICATIONS

Besides the obvious application of making precision and semi-precision clock measurements, a DDS clock measurement module can be used for other measurements as follows:

High-Resolution Frequency Counter: The module could be configured for use as a high-resolution frequency counter.

Embedded Applications: A DDS clock measurement circuit could be embedded into a product such as a GPS

timing receiver to provide high-resolution phase measurements at low complexity and cost.

Two-Port Network Measurements: The module can also be used to measure the phase stability of a passive or active two port network with the test setup shown in Figure 11. This setup is similar to that of a coherent noise test except that the device under test (DUT) is inserted into the signal path. For example, the DUT may be placed in a temperature chamber to measure its phase sensitivity to temperature.

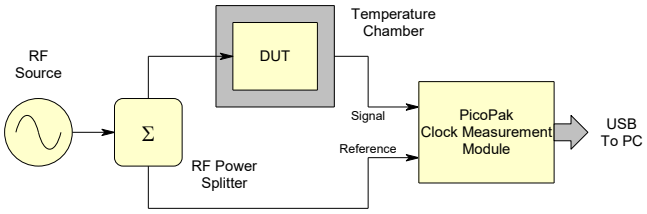

Figure 11. Two-Port Measurement Setup

ADVANTAGES AND LIMITATIONS

The primary advantages of the DDS clock measurement concept are its simplicity, small size, low power and low cost. It is also capable of making measurements at a relatively high rate. It is an example of combining hardware, firmware and software to replace traditional more complex hardware.

The principle limitations of the concept are somewhat limited frequency range and resolution. Another factor is a somewhat limited ability to track a rapidly changing frequency. It also operates by an unfamiliar method.

Extending the operating range toward lower frequencies is easy, but comes at the expense of lower resolution unless the DDS operates at a multiple of the input signal frequency. Extending the operating range toward higher frequencies is also feasible, within the range of DDS technology or via prescaling. Means for improving resolution have already been suggested.

CONDENSED SPECIFICATIONS

Condensed specifications for the DDS Clock Measurement Module are shown in Table I.

Table I. DDS Clock Measurement Module Condensed Specifications

Parameter		Specification
Frequency Range		5 MHz to 15 MHz
Resolution	Phase	6.1 ps at 10 MHz
	Frequency	$1x10^{-11}$/second
Noise		$<1.5x10^{-11}\tau^{-1}$
Frequency Accuracy		$<1x10^{-15}$
Frequency Slew		$\leq 3x10^{-7}$/s
Temperature Sensitivity		5 ps/°C typical
Signal & Reference Inputs		Sinewave +7 dBm 50 Ω
Interface		USB data, control & power
Data Streams		5 formats, at 10 ms & 1 s
Power		< 0.5 W
Size (LxWxH)		3.28”x2.25”x1.03”
Weight		< 5 oz

CONCLUSIONS

Several DDS clock measurement modules have been built and tested with consistent results, requiring no adjustments or calibration. There have been no significant problems with either acquisition or tracking. The modules seem quite immune to external interference, outliers are practically non-existent, and the user interface is easy to use. Runs of a month or more are generally glitch-free, especially if the host computer is a laptop or on an UPS. Frequency inaccuracy is at the $pp10^{16}$ level based on long coherent runs. The modules seem particularly well-suited for making continuous measurements of rubidium oscillators against a GPS timing receiver at sampling times of 10 seconds and longer. Their resolution and noise floor is adequate for measuring the long term stability of even very high performance sources.

The DDS clock measurement concept has been proven viable, and is an effective technique for making precise phase measurements.

ACKNOWLEDGMENTS

The author wishes to again acknowledge Mr. Tom Van Baak for suggesting the DDS clock measurement concept, and for his beneficial comments and suggestions about its implementation, along with those of Mr. John Miles and Mr. Ken Lyon.

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