A Frequency Error Multiplier for the PicoPak

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• Introduction
This paper describes a frequency error multiplier (FEM) that provides an order-of-magnitude resolution enhancement for a PicoPak clock measurement module [1], lowering its white PM noise floor to $2 \times 10^{-12} \tau^{-1}$.

The experimental FEM breadboard is divided into three sections, two phase-locked oscillator multipliers (PLOMs) and one mixer section, as shown in Figure 1. The unit accepts 10 MHz signal and reference inputs and produces a x10.625 error-multiplied output at 10.25 MHz.

• Background
A classic frequency error multiplier multiplies the input signal by a factor of 10 and the reference by a factor of 9, and then mixes them back to the nominal input frequency to provide an enhancement of the phase and frequency error by a factor of ten [2]. The Tracor Model 527 Frequency Difference Meter (see Figure 2) is an example of an instrument that used this concept [3]. Its error multipliers operate at 1 MHz and up to four stages can be cascaded (see Figure 3).

The author has designed and built several devices of that type over a period of some 50 years, generally based on a phase-locked oscillator multiplier (PLOM) as the basic building block [4]. Some of these devices used sampling phase detectors, but today IC PLL chips are generally used. Lowest noise is obtained by using a voltage-controlled crystal oscillator (VCXO). The PLL bandwidth must be sufficient to support measurements at the shortest sampling interval desired and to suppress the VCXO noise so that it follows the input signal variations. The bandwidth is ultimately limited by the spurious-free pulling range of the VCXO.
A fundamental constraint for frequency error multiplication is that instrumental noise sources are also enhanced, thus limiting the maximum useful multiplication factor. But another issue can be more important, coherent phase interference between the various stages resulting in spurious low frequency beats (phase ripple), thereby requiring careful attention to shielding, isolation and filtering, and the attendant complexity, narrow bandwidth, and phase temperature sensitivity and drift.

- **Requirements**

The requirements for this application are relatively modest, to provide resolution enhancement of at least x10 for a PicoPak clock measurement module while introducing minimal additional noise and TC. In particular, the error-multiplied PicoPak noise should still be limited only by its inherent phase quantization of about 6.1 ps at 10 MHz. The nominal reference and signal inputs should be 10 MHz. A further requirement is that the nominal error-multiplied output frequency be between 5 and 15 MHz, preferably near 10 MHz, and not significantly below 10 MHz since that would cause lower resolution. One constraint that need not be imposed is that the nominal output frequency be exactly 10 MHz, nor that the error multiplication factor be exactly 10 (or, indeed, any “even” value). The PicoPak does not require a “standard” signal input frequency, and its software can handle an “oddball” nominal frequency and error multiplication factor. As a practical matter, the multiplied reference and signal frequencies must be implementable with inexpensive, off-the-shelf available and low noise VCXOs, and are not necessarily or optimally the obvious values of 100 MHz and 90 MHz for 10 MHz inputs and outputs for an error multiplication factor of 10.

The input and output signal levels should be nominally the same as for the PicoPak. In particular, a PicoPak signal level of about +4 dBm has been found optimum for lowest noise.

- **Design**

The acceptability of “nonstandard” PLOM VCXO frequencies offers an important advantage for minimizing problems with coherent phase interference by using frequencies that are not 10 MHz multiples, and by using a nominal output frequency that is also not 10 MHz. More specifically, based on Abracon ABLJ0-V-series VCXO availability [5], a 96.00 MHz multiplied reference frequency, a 106.25 MHz multiplied signal frequency, and a resulting 10.25 MHz output frequency and x10.625 error multiplication factor were selected for this design. This improves the PicoPak phase resolution from 6.10 ps at 10 MHz to 0.56 ps at 10.25 MHz with the FEM. A block diagram of the frequency error multiplier system is shown in Figure 4.

The main disadvantage of using nonstandard PLOM VCXO frequencies is that FEM stages cannot be cascaded. It is unlikely, however, that multiple stages of frequency error multiplication would be useful with the PicoPak clock measurement module.
Based on previous 100 MHz and 125 MHz PLOM designs, an Analog Devices ADF4001 PLL device [6] was chosen as the PLL device.

The overall error multiplier is partitioned into three sections, the two PLOMS and the mixer/output section, each individually shielded, with 3.3V low-noise LT1761-3.3 LDO regulators [7] in the PLL sections. Each PLOM supply current is about 25 mA at +5 VDC and the mixer section draws about 50 mA at 7.5 VDC.

A Mini-Circuits ADE-1+ DBM [8] was selected as the mixer for this application. The photograph at the right shows its construction.

Other devices include LMV7219 comparators [10], PIC12F508 microcontrollers [11], and LMH6609 wideband amplifiers [12] (later replaced by OPA695s [18], see Addendum 1).

- **Circuit Schematics**

Schematics for the frequency error multiplier PLL and mixer sections are shown in Figures 5 and 6. The circuits have modest complexity and a single-quantity material cost under $200. All parts are available from stock at Digi-Key, Mouser and Mini-Circuits.
Figure 5. Frequency Error Multiplier PLL Section (1 of 2)
Figure 6. Frequency Error Multiplier Mixer Section

The initial schematic and PWB layout used a Mini-Circuits SCLF-10 10 MHz low pass filter after the mixer. This device has excellent attenuation properties but was found to have an unacceptably large phase TC at 10 MHz ($\cong 20 \text{ ps/}^\circ\text{C}$) and was therefore replaced with a simple 3-element LPF like that used in the PicoPak distribution amplifier [13].

- Packaging Options

The frequency error multiplier is divided into three $2.500'' \times 1.225''$ sections (two essentially identical PLOM sections and one mixer section), all implemented on a single $3.800'' \times 2.500''$ 2-layer board as shown in Figures 7 and 10. It is intended to be cut into three pieces and each section mounted in a Bud CU-123 die-cast aluminum box [14], thereby providing shielding between them. The boards are mounted inside the boxes with short #4 aluminum spacers at their four corners. Long straight Amphenol 132291 [15] PCB mounted SMA jacks are installed at the bottom of the boards and protrude from the bottom of the boxes, which are horizontally-mounted upside-down to a $4'' \times 6''$ aluminum plate with $1/8''$ #4 aluminum spacers (Mouser P/N 761-1107-4-AL-7) and $5/16''$ #4 screws, as shown in Figures 8 and 9 (the box covers are not used). The board width comfortably fits into the bottom of the slightly-tapered box (see Figure 11). The SMA connector pins fully engage the board pads, and their exposed length above the box is generous. The spacer connector pins fully engage the board pads, and their exposed length above the box is generous.
their tapped holes in the box (see Figure 12). DC power is supplied via feedthru capacitors in the box side walls. Drilling drawings for the PLL and Mixer boxes are shown in Figures 15 and 16.

Several other packaging options are feasible, including (a) using the three bare board sections, (b) using the uncut 3-section board (perhaps with shield partitions), (c) stacking the three boards (with right angle SMA connectors and perhaps with shields between them), and (d) packaging the three board sections vertically in a 3-compartment housing (perhaps with a motherboard and modified boards with connectors for their non-RF leads (e.g., power, lock, and reset). Ultimately it was found that, because of the frequency plan, a single-board design is feasible. A view of the overall frequency error multiplier mechanical assembly is shown in Figures 8 and 9. Additional packaging photos are shown in Figures 11-14.

Figure 7. Frequency Error Multiplier Board Layout
(Note that the mixer section in this layout uses the SCLF-10 LPF)
Figure 8. Overall Assembly Layout

Figure 9. Overall Assembly Hardware
The experimental mixer board shown in Figure 14 had the original Mini-Circuits SCLF-10 low pass filter layout and was modified to use the discrete component version.
Power connections are made to the three boards via 1500 pf feedthrough capacitors (Mouser P/N 800-24993X5S0152MLF). DC ground returns are via metal-to-metal grounds lugs under the feedthrough capacitors, and RF grounding is via metal-to-metal SMA connector hardware to the box and soldered to the board ground plane. Additional box grounding is provided by the four corner mounting screws on each board.

![Figure 15. PLOM Box Bottom Drilling Drawing](image)

![Figure 16. Mixer Box Bottom Drilling Drawing](image)

- **VCXO Tuning Characteristics**

The tuning characteristic of the two VCXOs were measured open-loop as shown in Figure 17. Values of +3.78 and +6.84 kHz/V were determined for the 96.00 and 106.25 MHz VCXO respectively. These tuning sensitivities are larger (much larger for the latter) than the +2.7 kHz/V slope implied by the ABLJO-V datasheet, and their unit-to-unit variability is unknown. The actual measured slopes were used to design the PLL loop filters.
### PLL Loop Filters

The AD4001 PLL RC loop filters (C1, R1 & C2) were designed using the excellent ADISimPLL program [16]. A target loop bandwidth of 500 Hz was used along with a nominal 45° phase margin for both PLLs, charge pump current settings were selected for suitable component value ranges, and the closest-available standard component values were then chosen. The resulting PLL loop filter parameters are shown in Table I. They are quite similar because the higher gain of the 96 MHz loop due to its lower N divider factor is compensated for by its lower K_v and charge pump current.

#### Table I PLL Parameters

<table>
<thead>
<tr>
<th>Freq</th>
<th>R</th>
<th>N</th>
<th>K_v</th>
<th>CP R_set</th>
<th>CP Cur</th>
<th>BW</th>
<th>φ Mar</th>
<th>C1</th>
<th>R1</th>
<th>C2</th>
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</thead>
<tbody>
<tr>
<td>MHz</td>
<td>Div</td>
<td>Div</td>
<td>kHz/V</td>
<td>KΩ</td>
<td>mA</td>
<td>Hz</td>
<td>°</td>
<td>nF</td>
<td>kΩ</td>
<td>nF</td>
</tr>
<tr>
<td>106.25</td>
<td>40</td>
<td>425</td>
<td>+6.84</td>
<td>4.75</td>
<td>3.71</td>
<td>010</td>
<td>530</td>
<td>51</td>
<td>1.0</td>
<td>130</td>
</tr>
<tr>
<td>96.00</td>
<td>10</td>
<td>96</td>
<td>+3.78</td>
<td>4.75</td>
<td>0.618</td>
<td>000</td>
<td>492</td>
<td>44</td>
<td>1.0</td>
<td>150</td>
</tr>
</tbody>
</table>

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![VCXO Tuning Characteristic](image)

96.00 MHz VCXO

![VCXO Tuning Characteristic](image)

106.25 MHz VCXO

Figure 17. VCXO Tuning Characteristics

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106.25 MHz PLL

96.00 MHz PLL

PLL Loop Filter Schematics (Ignore MUXOUT)
• PLOM Firmware

The AD4001 PLL chip for each PLOM is programmed at power on or reset by its associated PIC12F508 microcontroller. The firmware is written in C using the Microchip MPLAB X IDE and XC8 compiler, and the resulting hex code is loaded into the PIC with the Microchip IPE. The code is essentially the same for the two PLOMs except for the detailed divider and charge pump settings. The microcontroller goes into sleep mode to minimize noise after initially loading the PLL chip. The C source code for the 106.25 MHz PLOM is shown in Appendix I, and the code for the 96 MHz PLOM is similar.

• PLL Transient Response

The transient response of the two PLLs was measured by making a ≈ +1.8 kHz step change in their 10 MHz reference inputs, and is compared with the ADISimPLL predictions as shown in Figures 18 and 19. The transitions are nice with a single well-damped overshoot and take about 1 ms, in very good agreement with the predictions. Lockup is essentially instantaneous after application of either 10 MHz reference or 5 VDC power.
• VCXO Output Spectra

The output spectra of the two PLLs are clean without visible spurii, including those at their phase detector reference frequencies, and without any obvious close-in noise pedestal, as shown in Figures 15 and 16. These spectra were measured directly at the VCXO LVCMOS outputs via a 500 Ω series resistor into the 50 Ω spectrum analyzer input. The final design uses 300 Ω series resistors and the power delivered to a 50 Ω load is -2 dBm. If the VCXO output is unterminated at the input of the overall unity gain isolation amplifier, it delivers 0 dBm to a 50 Ω load (e.g., mixer input).

Figure 20. 106.25 MHz VCXO Output Spectra

Figure 21. 96.00 MHz VCXO Output Spectra

Feedthrough of the 10 MHz reference input was <90 dBc with respect to the PLOM outputs.

• Mixer Section

The mixer section (see Figure 6) comprises a pair of LMH6609 wideband op amp isolation amplifiers, an ADE-1 DBM mixer, an N=3, 1 dB ripple, 50 Ω Chebyshev low pass filter with a 15 MHz cutoff and an LMH6609 output amplifier that produces the desired 10.25 MHz error-multiplied output as the difference between the 106.25 MHz and 96.00 MHz PLOM signals. The LMH6609 devices require a supply voltage of at least 6.6 VDC, and 7.5 VDC is used.
The frequency and phase response of the LPF are shown in Figure 22.

Frequency Response
Phase Response

Figure 22. Frequency and Phase Response of 15 MHz Low Pass Filter

- **Frequency Error Multiplier 10.25 MHz Output Spectrum**

The spectrum of the 10.25 MHz FEM output is shown in Figure 21. The feedthrough of the 10 MHz reference is below -80 dBc, and that of the 96.00 MHz and 106.25 MHz components is -70 dBc and -58 dBm respectively. There were no visible spurs close to the carrier, and at least -80 dBc down in the span between 5 and 15 MHz. No harmonics of 10 MHz were visible, and the 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics of the 10.25 MHz output were -62 dBc and -52 dBc respectively.

1 MHz Span
100 kHz Span

Figure 21. 10.25 MHz FEM Output Spectra

- **Frequency Error Multiplier Output Level**

The 10.23 MHz output level from the mixer section of the frequency error multiplier was lower than initially expected (+1 dBm) because of the need to add a resistor in series with the VCXO LVCMOS outputs and the limited gain of the LMH6609 isolation amplifiers at 100 MHz (\(\approx A_v=2\), overall unity 50 \(\Omega\) matched gain). An ideal +4 dBm output was obtained by reducing the 10.25 MHz amplifier output series resistor to 25 \(\Omega\). An external LMH6609 RF amplifier was available to try higher PicoPak signal inputs up to +10 dBm but that made no significant difference. Substitution of wider-bandwidth OPA695 amplifiers can improve this (see Addendum 1).
• Initial Checks

The basic frequency error multiplication and scale factor were confirmed by making small frequency steps with a 48-bit DDS near 10 MHz, and by observing that the uncorrected 1-second ADEV reading of a pair of LPRO rubidium frequency standards was about $1 \times 10^{-10}$, ten times larger than actual.

A rough phase scale check was done with an adjustable coaxial air line phase shifter as shown in Figure 22A.

A more precise frequency scale factor check is shown in Figure 22B, where the DDS step size was $0.4263 \mu$Hz, $1.7036 \times 10^{-10}$ at 10.25 MHz, and the measured value was $1.702 \times 10^{-10}$ averaged over about 2 hours (the absolute frequency offset is caused by the different DDS and PicoPak/FEM references).
• **Coherent Noise Test**

The FEM was subjected to a coherent noise test with a standard PicoPak module. Identical 10 MHz signals were applied to both PLOM inputs and the PicoPak reference input, and the 10.25 MHz FEM output was applied to the PicoPak signal input. After correction for the FEM multiplication factor and frequency, the resulting coherent noise floor is shown in Figure 23. The 1 second ADEV is about 2.0x10^{-12} instead of the normal 1.4x10^{-11}, an order-of-magnitude improvement over the basic PicoPak. There is no significant interference visible on the All Tau stability plot, which shows pure white PM noise that integrates down as $\tau^{-1}$.

![Figure 23. PicoPak/FEM Coherent Noise Floor](image)

• **Absolute Frequency Tests**

The absolute frequency readings of the FEM-enhanced PicoPak were confirmed at both zero (coherent) and finite frequency offsets, the latter using known values from a 48-bit DDS and by comparison to a MilesDesign TimePod [17] clock measuring system.
RFS Measurement

The FEM was used with a PicoPak to compare two LPRO Rb oscillators. Without the FEM, the PicoPak has insufficient resolution and too high a noise floor to properly measure these devices in the short term region (1-100 seconds). With the FEM, these sources can be meaningfully measured. As shown in Figure 24, the short-term stability follows a white FM noise characteristic as expected for rubidium frequency standards, with a 1-second value of $1 \times 10^{-11}$ which is below the noise floor of a PicoPak without frequency error multiplication. The overnight 1s frequency record was clean:

![Figure 24. Stability Plot Using PicoPak with FEM](image)

FEM Phase TC

The FEM temperature coefficient of was measured as $+1.4 \text{ ps/°C}$ over a temperature range from 7.5°C to 42.8°C as shown in Figure 25. The phase TC characteristic was smooth and monotonic. This is a very acceptable value.

![Figure 25. FEM Phase TC Record](image)

FEM Lock Range

The FEM PLL will remain locked for a signal frequency within the tuning range of the 106.25 MHz VCXO, greater than ± 50 ppm and much larger than practical for the PicoPak.

PicoPak Software

A new version of the PicoPak user interface supports its operation with the frequency error multiplier by applying the FEM 10.625 error multiplier factor and 10.25 MHz FEM measurement frequency to the phase data.
The revised PicoPak Windows® user interface adds a Use Frequency Error Multiplier checkbox to the PicoPak Module group in the Configure dialog box where FEM error multiplication can be selected as an option as shown in Figure 26, using parameters stored in the PicoPak configuration file.

The PicoPak phase resolution and scale factor depend on the signal RF carrier period, the 14-bit DDS phase offset word size and the FEM frequency error multiplication factor (1 without an FEM).

For FEM-enhanced PicoPak measurements, the Nominal Frequency on the main screen is automatically set to 10.25 MHz so that its DDS is set to the FEM output frequency. However the frequency display and phase/frequency data are scaled to the 10 MHz signal frequency.

- **Preliminary Specifications**

Preliminary specifications for the breadboard PicoPak frequency error multiplier are shown in Table II.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplication Factor</td>
<td>Frequency Error Expansion x10.625</td>
</tr>
<tr>
<td>Signal RF Input</td>
<td>Frequency 10 MHz +e, e ≤ ±2x10^-10 Δf</td>
</tr>
<tr>
<td></td>
<td>Waveform Sinusoidal</td>
</tr>
<tr>
<td></td>
<td>Level 0 to +10 dBm (+7 dBm nominal)</td>
</tr>
<tr>
<td></td>
<td>Impedance 50 Ω nominal</td>
</tr>
<tr>
<td></td>
<td>VSWR ≤ 1.5:1</td>
</tr>
<tr>
<td>Reference RF Input</td>
<td>Frequency 10 MHz</td>
</tr>
<tr>
<td></td>
<td>Waveform Sinusoidal</td>
</tr>
<tr>
<td></td>
<td>Level 0 to +10 dBm (+7 dBm nominal)</td>
</tr>
<tr>
<td></td>
<td>Impedance 50 Ω nominal</td>
</tr>
<tr>
<td></td>
<td>VSWR ≤ 1.5:1</td>
</tr>
<tr>
<td>RF Output</td>
<td>Frequency 10.25 MHz +10.625ε</td>
</tr>
<tr>
<td></td>
<td>Waveform Sinusoidal</td>
</tr>
<tr>
<td></td>
<td>Level +4 dBm nominal (PicoPak signal input)</td>
</tr>
<tr>
<td></td>
<td>Impedance 50 ohms</td>
</tr>
<tr>
<td>Noise</td>
<td>ADEV (white PM noise) ≤ 3x10^-12τ^-1 (2x10^-12τ^-1 typical)</td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>Phase versus Temperature ≤ 5 ps / °C (±2 ps / °C typical)</td>
</tr>
<tr>
<td>Power</td>
<td>Voltage +5 VDC and +7.5 VDC (single +5 VDC expected)</td>
</tr>
<tr>
<td></td>
<td>Current 25 mA and 50 mA typical (original design)</td>
</tr>
<tr>
<td>Connectors</td>
<td>RF (all) SMA Female</td>
</tr>
<tr>
<td>Physical (breadboard unit)</td>
<td>Size (LxWxH) 4”x6”x1.5” (excluding connectors, cables &amp; feet)</td>
</tr>
<tr>
<td></td>
<td>Weight 26 oz (final package size and weight TBD)</td>
</tr>
<tr>
<td>Software</td>
<td>Windows® User Interface Revised PicoPak user interface application</td>
</tr>
</tbody>
</table>
• **Applications**

Besides its obvious use for making precision clock phase and frequency measurements, especially in the short term where the instrumental white PM noise dominates, an enhanced PicoPak with a FEM can serve as a very high resolution phasemeter. For example, it can measure the phase TC of a device such as a filter or distribution amplifier at the picosecond level.

• **FEM Use with PicoScan**

The FEM is not intended for use with the PicoScan because the signal PLL will not relock to the same phase condition after channel switching.

• **Potential Improvements**

It would be desirable to use higher gain devices as the isolation amplifier stages between the VCXOs and mixer to raise the mixer LO drive level and overall FEM output level (e.g., TI OPA695). It would also be advantageous if the mixer section could operate from the same +5V supply voltage as the two PLOM sections. Satisfactory operation should be possible without as elaborate shielding as used here, and a one-board arrangement would probably be OK, perhaps in a format resembling the PicoPak and with USB power, and a single PIC could load both PLL chips. Somewhat higher single stage frequency error multiplication factor could be used by choosing higher VCXO frequencies. It would be nice to have the PLL unlock indicators visible from the outside.

• **Conclusions**

The frequency error multiplier described herein is an effective way to improve the noise floor and resolution of a PicoPak clock measurement module. The overall system complexity is still competitive with alternative approaches having comparable performance. The biggest limitation is that it requires that the signal source be at or very near 10 MHz. The use of nonstandard PLOM frequencies was shown to avoid problems with coherent interference in single-stage FEM schemes of this sort, and software can perform the necessary data scaling.
• References

7. Data Sheet, LT1761 Series 100 mA Low Noise LDO Micropower Regulators, Linear Technology, Milpitas, A 95035, Rev F.
9. Data Sheet, SCLF-10+ Low Pass Filter, Mini-Circuits, Brooklyn, NY 11235,
10. Data Sheet, LMV7219 7-ns 2.7-V to 5-V Comparator with Rail-to-Rail Output, Texas Instruments, Dallas, Texas 75265, June 2016.

File: A Frequency Error Multiplier for the PicoPak.doc
W.J. Riley
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19
Addendum 1

Substitution of OPA695 RF Amplifiers

The two original LMH6609 wideband op amps (U4 and U5 on the mixer board) were removed and replaced with wider-bandwidth OPA695 devices [18] that can support higher gain at 100 MHz (specified for a 400 MHz bandwidth at VG=8, an overall 50 Ω matched gain of 12 dB). This substitution provides higher RF and LO drives to the mixer (and FEM 10.25 MHz output. An additional advantage is that the OPA695 can be operated from a single +5 VDC supply. It has an identical SOT-23 package and pinout as the LMH6609 except for the addition of a /Disable pin which can be left open.

Replacing U4 and U5 made no difference in the +4 dBm FEM output level, so the original LMH6609 devices were working as expected at VG=2. Rising the LO amplifier gain to VG=8 did not change the output level either, but also raising the RF amplifier to VG=8 increased the FEM 10.25 MHz output to +7 dBm (still with R24=24.9 Ω). Changing that resistor to its properly-matched 49.9 Ω value results in a +4 dBm FEM output, which is the optimum PicoPak signal input level.

Note that at this point the U10 FEM output amplifier still used an LMH6609 so a +7.5 VDC supply voltage was still required. The FEM mixer section supply current was higher with the two OPA695 devices and the associated higher RF levels, 80 mA versus 50 mA.

The FEM phase TC was re-measured with the wider-bandwidth OPA695 amplifiers and found to be somewhat larger and of opposite sign, about -2.5 ps/°C, still a satisfactory value (see phase plot at right). The dominant factor may be RF isolation amplifier phase TC tracking. The LFP phase TC is known to be small and the PLL’s static phase error should be near-zero versus VCXO TC/tuning with their charge pump phase detectors.

The U10 output amplifier LMH6609 was then also replaced with an OPA695 and its overall matched gain was increased to 8 dB by changing R23 to 75 Ω. This became the “final” FEM breadboard configuration as shown in the schematic below. The entire FEM runs from a single +5 VDC supply, and the total supply current is 115 mA.

The PicoPak/FEM noise floor was unchanged at $2.0 \times 10^{-12} \tau^{-1}$ (see stability plot at right).
Revised Mixer Section Schematic
Addendum 2

Single Board Version of Frequency Error Multiplier

Based on the performance of the FEM breadboard, including the lack of coherent interference problems, a single board version was created as shown in the figures below. This version fits into a PicoPak-sized enclosure and becomes a USB-powered PicoMult accessory for the PicoPak clock measurement module. The front panel is identical to the PicoPak, with 10 MHz signal and reference SMA inputs and an unlock LED indicator. The rear panel has an SMA connector for the 10.25 MHz output and a Type B USB power connector.

Schematics for the single-board PicoMult circuits are shown below.
Addendum 3
PicoMult Noise Floor Measurements with TimePod

Additional noise floor measurements were made for the one-board PicoMult using a Miles Design TimePod 5330A Programmable Cross Spectrum Analyzer by applying coherent 10 MHz drive to the PicoMult signal and reference inputs and the TimePod reference input, and connecting the +5 dBm 10.25 MHz PicoMult to the TimePod signal input. The TimePod results do not reflect the PicoMult x10.625 frequency error multiplication factor and need to be scaled accordingly.

The TimePod ADEV time domain plot shows quasi-white PM noise having a slope near $\tau^{-1}$ and a 1-second value of $1.6 \times 10^{-12}$ which corresponds to a PicoMult noise floor of $1.5 \times 10^{-13}$, thereby confirming the goal that the FEM noise is below that of the PicoPak quantization noise. The ripples in the ADEV plot are caused by some form of cyclic interference that appears associated with the frequency source and its interface to the PicoMult (e.g., powerline/ground loop effects).

The TimePod phase noise frequency domain spectral plot shows a flat white PM noise characteristic at -90 dBc/Hz out to the FEM PLL bandwidth of 500 Hz, thereby also confirming the PicoMult noise type and PLL BW.

A domain conversion calculation confirms that a white PM noise level of -90 dBc/Hz at a carrier frequency of 10.25 MHz corresponds to a 1-second ADEV of $1.5 \times 10^{-12}$.

WJR
11/12/16
Appendix I

106.25 MHz PLOM Firmware
C Source Code

/***************************************************************************/
/*
/* PIC12F508 program to control ADF4001 PLL for 106.25 MHz VCXO PLOM
/* Used in Frequency Error Multiplier
/*
/* Flash LED
/* Set and load three PLL words
/* Sleep
/*
/* This implements a fixed O/P of 106.25 MHz from a 10 MHz reference
/* R=40, N=425
/* VCXO is Abracon ABLJO-V-106.250 MHz
/* Measured VCXO tuning sensitivity (Kv)is +6.84 kHz/V
/* Aim for PLL loop BW = 500 Hz & 45 deg phase margin
/* Use 4.75 kOhm CP set R and 1.875 mA nominal (1.86 actual) CP current
/* with CP bits = 010 Selected for low current & OK component values
/* ADIsimPLL Design106-3_pll of 10/18/16
/* C1=1.0 nF, R1=130 kOhm, C2=6.8 nF
/* BW=530 Hz, Phase Margin=51 deg
/*
/* Created October 18, 2016
/* Last revised October 18, 2016
/*
/* Hints: Remove programming connections to run
/* Runs best in one-shot sleep mode
/* Press reset button after programming to insure lockup
/*
/* W.J. Riley (c) Hamilton Technical Services, Beaufort, SC 29907
/*
/***************************************************************************/

// Includes
#include <xc.h>

// Macros
#define _XTAL_FREQ 4000000 // Internal 4 MHz oscillator

// CONFIG
#define OSC = IntRC // Oscillator Selection bits
#define WDT = OFF // Watchdog Timer Enable bit
#define CP = OFF // Code Protection bit
#define MCLRE = ON // GP3/MCLR Pin Function Select bit

// Function prototypes
void Flash_LED(void);
void Send_Data(void);

// Global variables
int i; // General index
int n=3; // Loop counter
unsigned short long PLL; // 24-bit PLL data word
```c
int main(void) {
    // Loop to load PLL chip n times
    // Replace n with 1 for continuous testing
    while(n) {
        // Set up I/Os
        // Inputs (1) = GP4, Outputs (0) = GP0, GP1, GP2, GP5
        // GP4 input is NC unless needed
        // GP0 Pin 7 is PLL serial data
        // GP1 Pin 6 is PLL serial clock
        // GP2 Pin 5 is PLL load enable
        // GP5 Pin 2 is LED (H=On)
        TRIS=0xD8;
        // Set up Option register
        // Must clear bit 5 to use GP2 Pin 5 as output
        OPTION=0xC0;
        // Flash LED
        // Omit for continuous load testing, or use as trigger
        Flash_LED();
        // Set and send Initialization word (Code 11) /*
        Bits   Setting    Description
        23-22  00        Don't care Reserved
        21  0          PD2 Power Down 2 normal
        20-18  010       CS2 Current Setting 2 1.86 mA w/ 4.75 kohm
        17-15  010       CS1 Current Setting 1 Ditto
        14-11  0000      TC Timer Control 3 cycles
        10-9   00        FL Fastlock disabled
        8  0          CP Normal Charge Pump output
        7  1          P Positive PD polarity
        6-4   001       MUX Digital lock detect O/P
        3  0          PD1 Power Down normal
        2  0          CR Counter Reset normal
        1-0   11        CB Initialization word code

        Positive PD (VCXO freq up with increasing CV)
        Initialization word = 0000 1001 0000 0000 1001 0011 = 0x090093
        For R divider mux O/P, = 0000 1001 0000 0000 1010 0011 = 0x0900A3
        For N divider mux O/P, = 0000 1001 0000 0000 1100 0011 = 0x0900C3
        For Serial Data mux O/P, = 0000 1001 0000 0000 1110 0011 = 0x0900E3 */

        PLL=0x090093;
        Send_Data();

        // Set and send Reference word (R=40) (Code 00) /*
        Bits   Setting    Description
        23-21  000        Don't care Reserved
        20  1          LD Lock Detector 5 cycles
        19-18  00        TM Test bits normal
        17-16  00        AB Antibacklash 3 ns
        15-2   R 14-bit R counter = 40 dec = 0x28 hex = 00000000101000
        1-0   00        CB Reference counter word code
```
Reference word = 0001 0000 0000 0000 1010 0000 = 0x1000A0
*/

PLL=0x1000A0;
Send_Data();

// Set N Counter word (N=425)
// Set and send N-Counter word (Code 01)
/*
Bits    Setting Description
23-22   00      Don't care Reserved
21      0       CP Charge pump gain setting 1
20-8    N 13-bit B counter = 425 dec = 0x1A9 hex = 0000110101001
7-2    Don't Care Not Used
1-0    01      CB N-Counter word code

N Counter word = 0000 0001 1010 1001 0000 0001 = 0x01A901
*/

PLL=0x01A901;
Send_Data();

// Decrement counter
n--;
}

// Loop done
SLEEP();
}

// Function to flash LED at GP5 pin 2
void Flash_LED(void)
{
    // Turn on the Pin 2 LED
    GP5=1;

    // Delay for 0.1 second
    __delay_ms(100);

    // Turn off the Pin 2 LED
    GP5=0;
}

// Function to send 24 bits to PLL
// The 24-bit word is PLL
// Data = GP0 pin 7
// Clock = GP1 pin 6
// Load Enable = GP2 pin 5
void Send_Data(void)
{
    // Send the 24-bit tuning word
    for(int i=0; i<24; i++)
    {
        // Send PLL bits MSB first
        if(PLL & (1UL << (23-i))) // Is data bit 1?
        {
            // Set data line to 1
            GP0=1;
        }
    }
}
else // Data LS bit is 0
{
    // Clear data line to 0
    GP0=0;
}

// Settling delay
__delay_us(10);

// Send clock pulse
GP1=1;
__delay_us(10);
GP1=0;

// Settling delay
__delay_us(10);

// Pulse the load enable line
GP2=1;
__delay_us(10); // 10 us normal, 100 us for continuous testing
GP2=0;